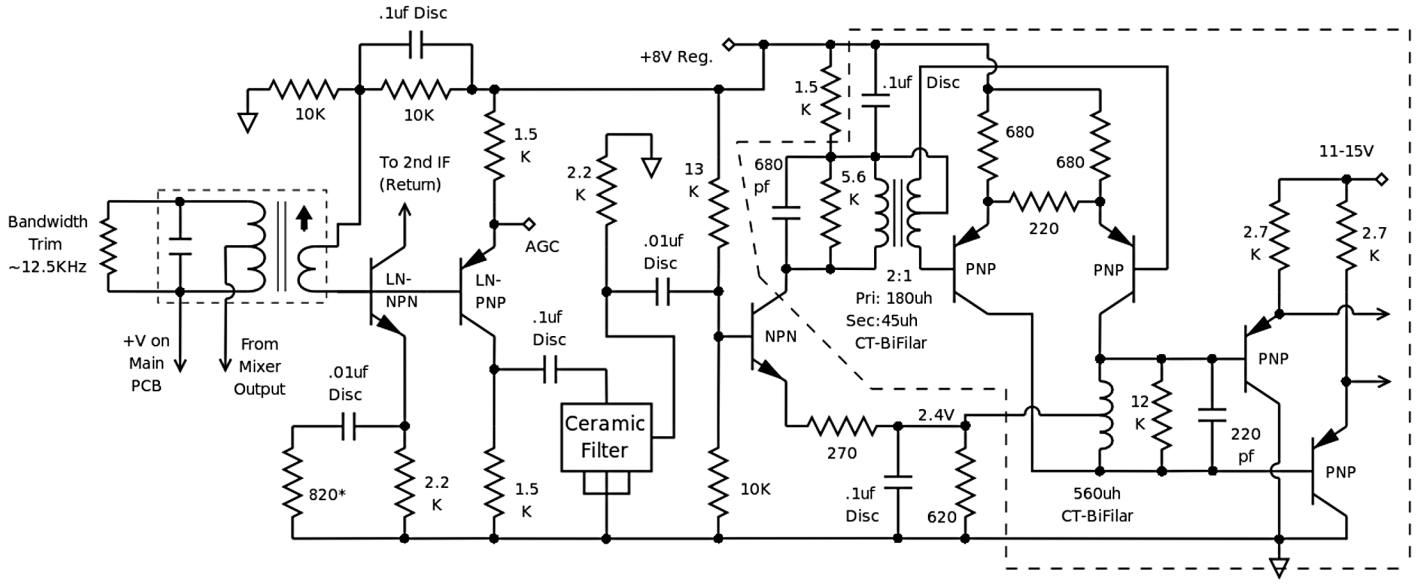
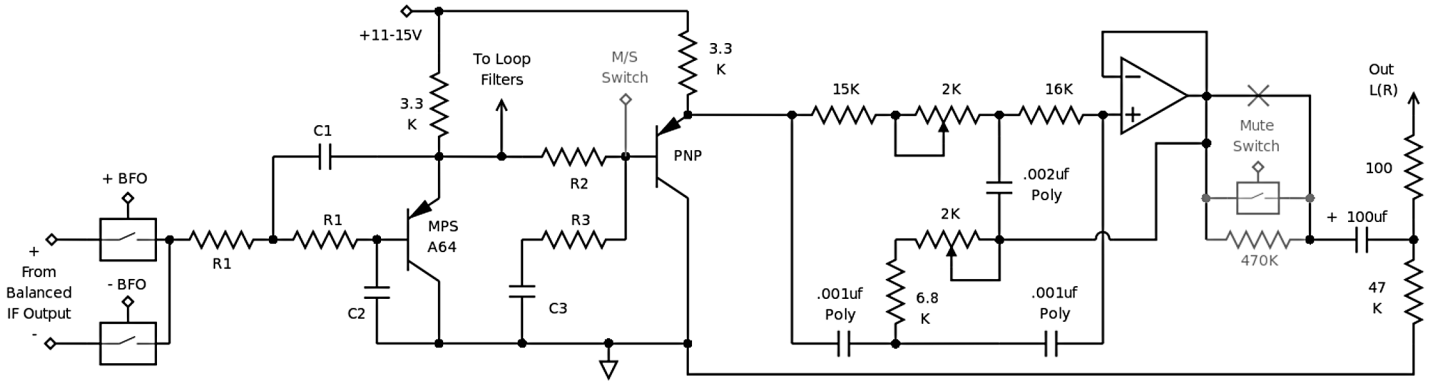
Discrete QuAM Detector for AM Stereo

The following schematic shows the IF processing section. It takes the IF signal from the open collector of the mixer output and returns an open collector signal back to the main IF section on the tuner. AGC is applied to the signal prior to the ceramic filter. Post filter amplification provides ~52db of gain with low impedance output to drive the synchronous detector switches. The components within the dotted area comprise the circuit to amplify and buffer the output and could be replaced with a high performance dual Op-Amp that would output a 6Vp-p signal at 450KHz.

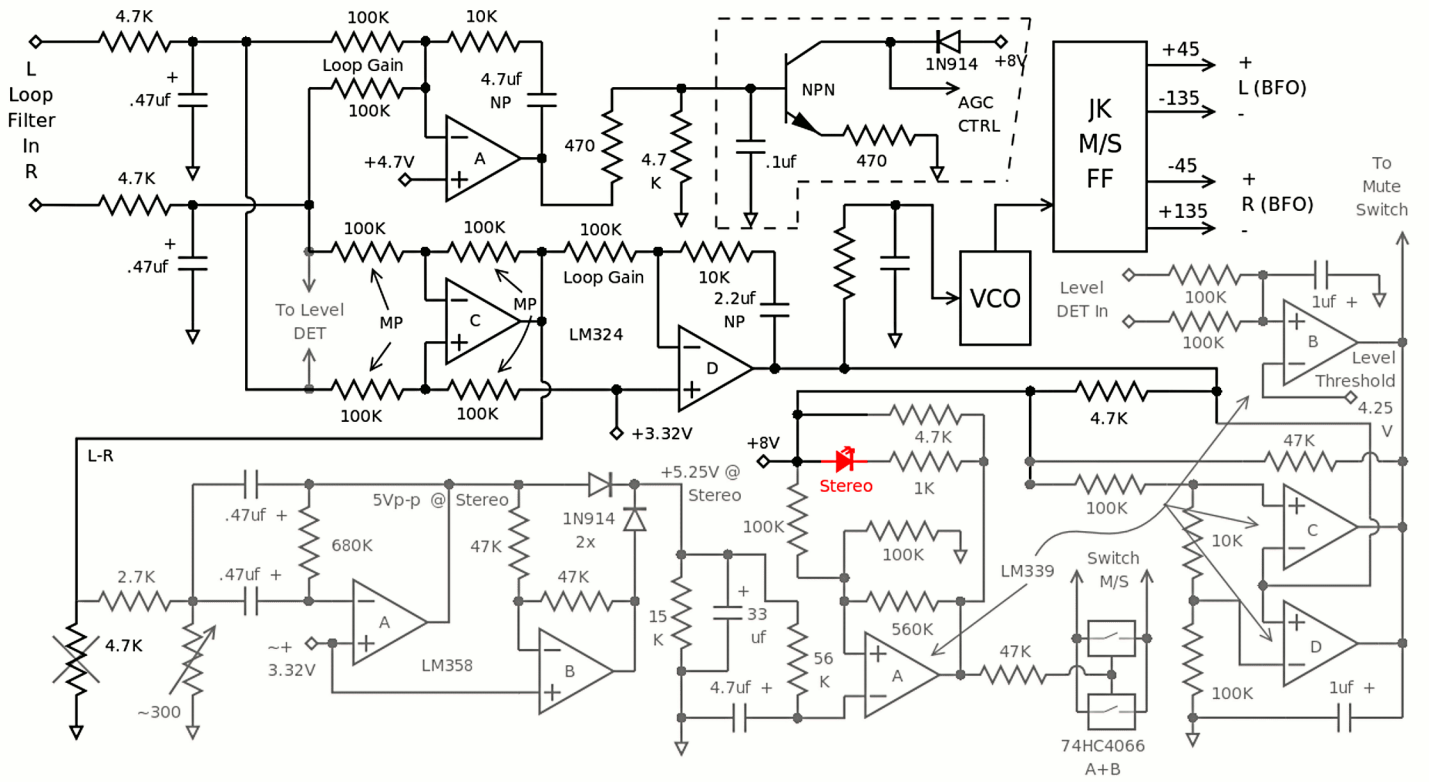


The next schematic does the synchronous detection, NRSC de-emphasis, 10KHz notch filter and equalization to flatten out the response. The synchronous detection is preformed with a quad analog switch (CD74HC4066) which is fed into an 2nd order Chebychev filter to remove the IF harmonic components and provide a ~+9db boost for the upper audio frequencies to help compensate for RF & IF filter attenuation. A good output Op-Amp would be a MC34072.



+/- 7.5 KHz Cerami c Filter	+/- 10KHz Ceramic Filter	+/-12.5KHz Ceramic Filter	+/- 15KHz Ceramic Filter
R1=17K C1=.0068uf Poly	R1=15K C1=.0068uf Poly	R1=13K C1=.0068uf Poly	R1=12K C1=.0068uf Poly
R2=3.6K C2=180pf Poly	R2=3.9K C2=180pf Poly	R2=3.9K C2=180pf Poly	R2=3.9K C2=180pf Poly
R3=5.1K C3=.01uf Ploy	R3=4.7K C3=.01uf Poly	R3=5.1K C3=.01uf Poly	R3=5.6K C3=.01uf Poly

The next schematic is the BFO with PPL, AGC processing and the grayed out components depict the optional pilot detection with Stereo ID along with PLL lock detector and signal level detector for muting when detector is out of lock and/or weak signal conditions.



The L & R signals are filtered to pass 72Hz and lower frequencies. For AGC the signals are summed at the input of loop amp with a corner frequency of 3.38Hz. The output is fed into an NPN transistor that controls the current through the 1N914 diode varying its resistance with the current thus varying the swamping of the IF amp driving the ceramic filter input. The components within the dotted lines need to be placed next to the IF amp. For the PLL VCO the L & R signals are sent to a differential amp to obtain L-R, the quadrature signal, which the PLL uses for the control voltage. The PLL loop filter corner frequency is set at 7.23Hz. For both AGC & PLL loop filters the loop gain is controlled by the 100K resistors. Adjustment of these (smaller) will reduce the lock time while increasing the potential for overshoot. A proper balance will yield fast lock with no overshoot. The VCO could be a top spec CMOS TLC555 timer which has an upper astable frequency range of 2.1MHz but this would be the pick of the crop since its minimum spec is 1.2MHz and 4*f=1.8MHz. The loop voltage is sent to the VCO operating at 4*(IF Frequency) so the ÷4 JK Master/Slave Flip-Flop will generate BFO signals in perfect quadrature. These are fed into the quad analog switches to detect the L & R signals. If the optional circuitry (depicted as grayed out) is used L-R is passed through a bandpass amp centered a 25Hz with a Q of 25.1 and A=126 for pilot detection. It is then full wave rectified and filtered to provide a t=rc=260ms delay so that comparator 'A' with hysteresis points at 63.2% and 36.8% can minimize excessive mono/stereo switching during marginal signal conditions. The PLL loop volts are also passed through a window detector using comparators 'C' & 'D' for lock detection along with a threshold level detector using comparator 'B' to control the muting of the signals during poor or no signal conditions. If the 0 signal level is at 4.2V and full strength at 4.7 then the threshold could be set at ~10% e.g. 4.25V for starters.

NOTES:
All NPN & PNP transistors are 2N3904 & 2N3906 respectively or equivalent.
The LN-NPN & LN-PNP transistors could be MPSH10 & MPSH81 respectively or equivalent.
The unused amp 'B' in the LM324 chip will need to have its (-) input connected to its output and the (+) input connected to a reference voltage e.g. 3.32V. This amp is available for use if needed for some other purpose.